REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 106-110, 112-116, 119, 120, 123, 126-129, 136 and 139-155 are pending; Claims 120 and 136 have been currently amended; Claims 152-155 have been newly added; Claims 1-105, 111, 117, 118, 121, 122, 124, 125, 130-135, 137 and 138 have been canceled.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 106-110, 112-116, 119, 141, 142 and 154

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As previously presented, independent Claim 106 is recited below:

106. A semiconductor chip or wafer comprising:
a silicon substrate;
a metallization structure over said silicon substrate;
a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material;
a polymer layer over said passivation layer, wherein said polymer layer has a thickness of between 2 and 50 μm; and
a metal trace over part of said polymer layer and over said first contact pad, wherein said metal trace comprises a gold layer with a thickness of between 2 and 100 μm, and wherein said metal trace comprises a second contact pad connected to said first contact

pad, wherein the positions of said first and second contact pads from a top perspective view are different.

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Reconsiderations of Claims 106, 107-110, 112, 113, 116, 119, 141 and 142 rejected under 35 U.S.C. 102(e) as being anticipated by Leu et al. (US 6,605,549), and of Claims 114-115 rejected under 35 U.S.C. 103(a) as being unpatentable over Leu et al. in view of Kikuchi (US 2003/0102551) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip or wafer claimed in Claim 106 patentably distinguishes over the citation by Leu et al. (US 6,605,549).

Leu et al. teaches a circuit component comprising a semiconductor substrate 40; a polymer layer 42 over said semiconductor substrate 40; and a metal layer 53 over said semiconductor substrate 50 and over said polymer layer 42.

The Examiner considers reference number of "53" can be analogous to "metal trace". ~ *See lines 4-10 of page 3, in the last Office Action mailed Mar. 14, 2007* ~

Applicants respectfully traverse the Examiner's opinion because reference number of "53" can not be analogous to "metal trace". Leu et al. teaches a metal layer 52 is formed over all over the top surface of said semiconductor substrate 40. The metal layer 52 has no pattern with a trace. Reference number of "53" indicates an "overburden", which will be removed by a chemical mechanical polishing (CMP) process. After the CMP process, only the metal layer 52

in trenches 49A and 49B and in a via 48 is left. Only the left metal layer 52 in the trenches 49A and 49B has a pattern with a trace. Only the left metal layer 52 in the trenches 49A and 49B can be deemed as a metal trace. The left metal layer 52 in the trenches 49A and 49B has a thickness dramatically smaller than that of the 42. ~ See Fig. 4E; col. 10, lines 19-24 and 40-47 ~

Leu et al. fail to teach, hint or suggest that the left metal layer 52 in the trenches 49A and 49B may have such a thickness of between 2 and 100 μm, as claimed in Claim 106.

Withdrawal of rejection under 35 U.S.C. 102(e) to Claim 106 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 106 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 107-110, 112-116, 119, 141, 142 and 154 patently define over the prior art as well.

Response to Claims 120, 123, 126-129, 131, 143-146 and 155

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As currently amended, independent Claim 120 is recited below:

120. A semiconductor chip or wafer comprising:
a silicon substrate;
a metallization structure over said silicon substrate;
a passivation layer over said metallization structure, wherein an opening in said passivation layer exposes a first contact pad of said metallization structure, and wherein said passivation layer comprises an inorganic material;
a second contact pad connected to said first contact pad, wherein said second contact pad comprises a gold layer with a thickness of between 2 and 15 μm; and

a circuit interconnect wirebonded to said second contact pad.

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Reconsiderations of Claims 120, 123, 126-129, 131 and 143-145 rejected under 35 U.S.C. 102(e) as being anticipated by or under 35 U.S.C. 103(a) as being obvious over Kikuchi (US2003/010,2551), and of Claim 146 rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Leu et al. (US 6,605,549) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip or wafer claimed in Claim 120 patentably distinguishes over the citation by Kikuchi (US2003/010,2551).

Kikuchi teaches a circuit component comprising a silicon substrate 110; a metallization structure 120 over said silicon substrate 110; a passivation layer 130 over said metallization structure 120, wherein an opening in said passivation layer 130 exposes a first contact pad 120 of said metallization structure, and wherein said passivation layer 130 comprises an inorganic material; and a second contact pad (a portion of metal trace 150 and 160 under element 170) connected to said first contact pad 120, wherein said second contact pad (a portion of metal trace 150 and 160 under element 170) comprises a gold layer with a thickness of between 2 and 15 μm. *~ See Fig. 2 and para.[0039]-[0043] ~*

Kikuchi teaches said second contact pad (a portion of metal trace 150 and 160 under element 170) is used to have a bump 170 formed thereon, but fails to teach a circuit interconnect can be wirebonded to said second contact pad (a portion of metal trace 150 and 160 under element 170), as currently claimed in currently amended Claim 120.

Withdrawal of rejection under 35 U.S.C. 102 (e) to Claim 120 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 120 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 123, 126-129, 143-146 and 155 patently define over the prior art as well.

Response to Claims 136, 139, 140 and 147-153

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As currently amended, independent Claim 136 is recited below:

136. A circuit component comprising:
a semiconductor substrate;
a metallization structure over said semiconductor substrate;
a passivation layer over said metallization structure, wherein said passivation layer comprises an inorganic material;
a metal trace over said passivation layer, wherein said metal trace comprises a titanium-containing layer, a first gold layer on said titanium-containing layer, and a second gold layer on said first gold layer, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm, said first gold layer has a thickness of between 0.05 and 3 μm, and said second gold layer has a thickness of between 2 and 100 μm; and
a circuit interconnect wirebonded to said metal trace.

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Section I:

Reconsiderations of Claims 136 and 151 rejected under 35 U.S.C. 102(e) as being anticipated by Leu et al. (US 6,605,549) are requested based on the following remarks.

Applicants respectfully assert that the circuit component claimed in claim 136 patentably distinguishes over the citation by Leu et al. (US 6,605,549).

Leu et al. teaches a circuit component comprising a semiconductor substrate 40; a polymer layer 42 over said semiconductor substrate 40; and a metal layer 53 over said semiconductor substrate 50 and over said polymer layer 42.

The Examiner considers reference number of "53" can be analogous to "metal trace". ~ *See line 20 of page 4 through line 5 of page 5, in the last Office Action mailed Mar. 14, 2007* ~

Applicants respectfully traverse the Examiner's opinion because reference number of "53" can not be analogous to "metal trace". Leu et al. teaches a metal layer 52 is formed over all over the top surface of said semiconductor substrate 40. The metal layer 52 has no pattern with a trace. Reference number of "53" indicates an "overburden", which will be removed by a chemical mechanical polishing (CMP) process. After the CMP process, only the metal layer 52 in trenches 49A and 49B and in a via 48 is left. Only the left metal layer 52 in the trenches 49A and 49B has a pattern with a trace. Only the left metal layer 52 in the trenches 49A and 49B can be deemed as a metal trace. The left metal layer 52 in the trenches 49A and 49B has a thickness dramatically smaller than that of the 42. ~ See Fig. 4E; col. 10, lines 19-24 and 40-47 ~

Leu et al. fail to teach, hint or suggest that the left metal layer 52 in the trenches 49A and 49B may have such a thickness of between 2 and 100 μm, as claimed in currently amended Claim 136.

Furthermore, Leu et al. fail to teach, hint or suggest a circuit interconnect wirebonded to the left metal layer 52 in the trenches 49A and 49B, having a pattern with a trace, as claimed in Claim 136.

Withdrawal of rejection under 35 U.S.C. 102(e) to Claim 136 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 136 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 139, 140 and 147-153 patently define over the prior art as well.

Section II:

Reconsiderations of Claims 136-140 and 148-150 rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi (US2003/0102551), and of Claim 147 rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Leu et al. (US 6,605,549) are requested based on the following remarks.

Applicants respectfully assert that the circuit component claimed in Claim 136 patentably distinguishes over the citation by Kikuchi (US2003/0102551).

Kikuchi teaches a circuit component comprising a silicon substrate 110; a metallization structure 120 over said silicon substrate 110; a passivation layer 130 over said metallization structure 120, wherein said passivation layer 130 comprises an inorganic material; and a metal

trace 150 and 160 over said passivation layer 130, wherein said metal trace 150 and 160 comprises a titanium-containing layer, a first gold layer on said titanium-containing layer, and a second gold layer on said first gold layer, wherein said titanium-containing layer has a thickness of between 0.01 and 3 μm, said first gold layer has a thickness of between 0.05 and 3 μm, and said second gold layer has a thickness of between 2 and 100 μm.

~ See Fig. 2 and para. [0039]-[0043] ~

However, Kikuchi fails to teach, hint or suggest that a circuit interconnect can be wirebonded to said metal trace 150 and 160, as claimed in currently amended Claim 136.

Withdrawal of rejection under 35 U.S.C. 102 (e) to Claim 136 is respectfully requested.

For at least the foregoing reasons, applicants respectfully submit independent Claim 136 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 139, 140 and 147-153 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Le not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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